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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PATHAK, SHANTANU

ART UNIT

PAPER NUMBER

2829

NOTIFICATION DATE

DELIVERY MODE

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ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/581,335	Applicant(s) KUSUNOKI, KATSUKI	
	Examiner SHANTANU C. PATHAK	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-11 are pending in the instant application.
2. Applicant's reply, dated October 26th, 2009, is in response to the Examiner's office action, dated June 24th, 2009.

Response to Arguments

3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
5. Claims 1, 3-7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji in view of Araghi.

With respect to Claim 1, Shuji teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, comprising: a step of **linearly forming first grooves** in a desired chip shape by etching on a side of the gallium nitride compound semiconductor layers of said wafer (Paragraph 7, lines 1-6; Drawing 3, elements 11, 2, 3); a step of **forming second grooves** having a line width (W2) equal to or

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smaller than a line width (W1) of the first grooves on a side of the substrate of said wafer (Paragraph 7, lines 9, 10; Drawing 3, elements W1, 11, W2, 22); and a step of **dividing said wafer** along said first and second grooves into pieces each of a chip shape (Paragraph 7, lines 11, 12; Paragraph 10, lines 12-14; Paragraph 21, lines 9, 10) {The wafers are separated along the “Chuo Line”}.

Shuji does not explicitly teach the limitation **wherein** the second grooves are formed at positions not conforming to the central lines of the first grooves or the limitation **wherein** said positions at which the second grooves are formed are decided by performing a trial division in advance.

Araghi further discloses the limitation **wherein** the second grooves are formed at positions not conforming to the central lines of the first grooves (Column 3, lines 50-56; Fig. 3, elements 35, 37, 40, 44, 45).

While Shuji in view of Araghi does not explicitly teach the limitation **wherein** said positions at which the second grooves are formed are decided by performing a trial division in advance, Shuji in view of Araghi does teach the step of **linearly forming first grooves**, the step of **forming second grooves** and finally, the step of **dividing said wafer** along said first and second grooves (see above) {The process of linearly forming first grooves, forming second grooves and dividing said wafer along said first and second grooves for the purpose of optimizing the position of the second groove for subsequent duplication is not given patentable weight because where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) In addition, mere duplication of parts has

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no patentable significance unless a new and unexpected result is produced. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)}.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji with the groove positioning as taught by Araghi to provide chips having precisely controlled ends and line edges for butting against the ends of like arrays (Araghi).

With respect to Claims 3-5, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji in view of Araghi does not explicitly disclose: the limitation wherein the positions not conforming to the central lines of said first grooves are, when viewing the substrate in plan[e] view, positions parted by 20 to 100% of the line width (W1) of the first grooves relative to the central lines of the first grooves **[Claim 3]**; the limitation wherein at the step of forming said second grooves, the second grooves are formed so that the obliquely divided chips assume cut faces having angles in the range of 60 to 85° **[Claim 4]**; and the step of polishing the substrate side prior to forming the second grooves to adjust a thickness of the substrate in a range of 60 to 100 μm **[Claim 5]**. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to employ the limitations as described in Claims 3-5 of the instant application in the invention of Shuji in view of Araghi because “[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to

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discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

With respect to Claim 6, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji further teaches the limitation wherein said first grooves are confronted by an electrode-forming surface for forming an electrode for gallium nitride compound semiconductor chips (Para. 16; Fig. 4) {see explanation above}.

With respect to Claim 7, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji further teaches the limitation wherein said second grooves are formed by at least one method selected from the group consisting of etching, dicing, pulse laser and scribe (Paragraph 9, lines 1-3).

With respect to Claim 11, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. That the final product resultant from a method for the production of

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gallium nitride compound semiconductor chips is a gallium nitride compound semiconductor chip is inherent to the process.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji in view of Araghi as applied to Claim 1 above, and further in view of Tsuda and Yamasaki.

With respect to Claim 2, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji in view of Araghi does not teach the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface, said first and second grooves are formed respectively along a first direction parallel to an orientation flat and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves.

Tsuda teaches a method of producing a nitride semiconductor structure for employing in light-emitting devices. Tsuda further discloses the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface (Para. 57).

Yamasaki teaches a semiconductor laser device formed by a gallium nitride-based semiconductor. Yamasaki further discloses the limitation said first, 32, and second, 34, grooves are formed respectively along a first direction parallel to an orientation flat and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves (Paras. 86-92; Figs. 3-5).

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Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the substrate as taught by Tsuda and with the grooves as taught by Yamasaki to allow the growth of crystal structure on the substrate (Tsuda: Abstract) and to divide a wafer in accordance with forming a semiconductor laser device (Yamasaki: Para. 93), respectively.

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji in view of Araghi as applied to Claim 1 above, and further in view of Tanaka.

With respect to Claims 8-10, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. While Shuji in view of Araghi does not disclose: the limitation wherein said substrate is formed of hexagonal SiC **[Claim 8]**, the limitation wherein said substrate is formed of a hexagonal nitride semiconductor **[Claim 9]**, and the limitation wherein said substrate is formed of hexagonal GaN **[Claim 10]**, the limitations as disclosed in Claims 8-10 are considered as obvious variants.

Tanaka teaches a method of crystal growth of a III-V compound semiconductor composed of at least one group-III element, with the crystal being hexagonal in structure or a nitride semiconductor. Tanaka further discloses the similarities in crystal structure between sapphire and hexagonal SiC (Paragraph 138) **[Claim 8]**, hexagonal nitride semiconductor (Paragraph 19, lines 11-14) **[Claim 9]** and hexagonal GaN (Paragraph 19, lines 1-10) **[Claim**

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101. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the material surfaces as taught by Tanaka to understand crystal growth mechanisms of III-V compound layers for use in semiconductor device applications.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANTANU C. PATHAK whose telephone number is (571) 270-5727. The examiner can normally be reached on Monday-Thursday, 10:00 a.m.-4:00 p.m.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHANTANU C PATHAK/

Examiner, Art Unit 2829

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829